ROMANIAN JOURNAL OF INFORMATION SCIENCE AND TECHNOLOGY
Volume **12**, Number 3, 2009, 283–307

Single-Pole Double-Thru and True Time Delay Lines in Alumina Packaging Based on RF MEMS Switches in Silicon Technology

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Abstract. Packaged MEMS devices for RF applications have been modelled, realized and tested. In particular, RF MEMS single ohmic series switches have been obtained on silicon high resistivity substrates and they have been integrated in alumina packages to get single-pole-double-thru (SPDT) and true-time-delay-line (TTDL) configurations. For this purpose, the individual switches have been considered as the building blocks of more complicated structures, and the alumina substrate has been properly tailored in order to get the best electrical performances considering all the technological steps necessary for the final

hybrid device. Actually, several parameters and processes have been considered for such an optimization, involving the geometry, the wire bonding and the cover to be used. Test structures with technologically actuated switches have been also manufactured in order to have the best reference result for the proposed structures. After that, the same devices have been packaged for the final test. As a result, TTDLs for wide band operation, specifically designed for the (6–18) GHz band, have been obtained, with insertion losses less than 2 dB up to 14 GHz for the short path and 3 dB for the long path (5 dB for the real device), and delay times in the order of 0.3–0.4 ns for the short path and 0.5–0.6 ns for the long path. The maximum differential delay time is in the order of 0.2 ns.

Key words: RF MEMS, SPST, SPDT, TTDL, packaging.

1. Introduction

RF MEMS devices are currently considered a winning solution for many applications where mainly pin diodes have been utilized up to now [1]. True-time-delay-line (TTDL) as well as matrices or phase shifters can take advantage from the MEMS technology because of the extremely low loss, linear behaviour and virtually no current consumption in electro-statically actuated devices [2–6]. A number of issues are presently considered as mandatory for releasing the reliability of MEMS devices and configurations, including the mechanical performances and charging characteristics. One of the main items in considering RF MEMS switches reliable devices is the packaging. There are several examples in literature on how to solve efficiently such an issue, trying to protect the device for decreasing the contribution of different effects: (i) the increase in the insertion loss because of the additional transitions, (ii) the inert atmosphere needed for avoiding the sticking due to residual humidity and related leakage control, (iii) temperature contributions, (iv) radiation in case of special applications like space devices.

In this paper we present a possible packaging solution for MEMS switches in a TTDL configuration. It is based on individual RF MEMS switches embedded in an alumina package. Such a hybrid configuration is promising as it concerns with the optimization of a quite established technology on silicon or quartz for MEMS switches, to be married with technologies already developed on the usual substrates for high frequency applications, where feeding lines and packaging can be easily realized.

2. SPST and SPDT technology and test

MEMS single switches (SPST) have been obtained by means of an eight-mask process up to the release of the sacrificial layer by using the facilities at the FBK-irst foundry. A 525 μm thick, high resistivity silicon substrate has been used as a support for the successive technological steps, ended with the removal of a photoresist sacrificial layer to get a suspended gold membrane as a double clamped bridge. Such a device is actuated by means of an electrostatic potential provided by external

pads and polysilicon, highly resistive feeding lines. The diagram of the single switch used for the TTDL configuration is given in the following Fig. 1.

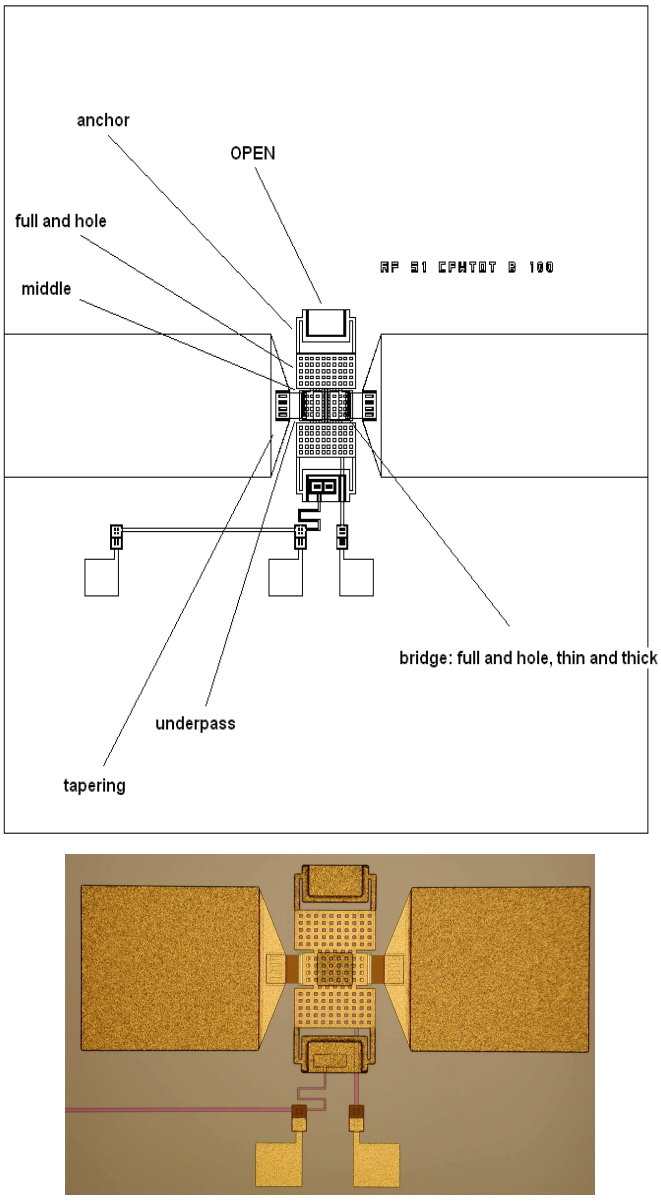

Fig. 1. Schematic diagram of the SPST developed for the TTDL structure and photo of the realized device.

In Fig. 2 is presented the scheme used for realizing the SPDT configuration. Actually, an alumina substrate has been worked out for obtaining holes where to place

the SPST previously cut from the silicon wafer. Three bonding wires connect the I/O lines of the SPST to the matched microstrip on the alumina substrate. Of course, several sources of electrical mismatch have to be considered, as also investigated by means of preliminary simulations: (i) the passage from one substrate to another one using bonding wires, (ii) the length of the wires and the relative height between the two substrates, (iii) the shape and possible related resonant effects of the location for the SPST, (iv) the necessity to have both SPST quite close each other, in order to optimize the SPDT electrical response, (v) the microstrip to CPW transition use for measurement purposes. An additional loss will be caused by the presence of the cover for the fully packaged structure. On the other hand, the above defined contributions are unavoidable for any packaged structure, and they are the major source of insertion loss, while the MEMS devices, not exceeding 0.4 dB of loss, are for sure less important; it helps in an effective decrease of the total insertion loss when configurations like TTDL with several bits are considered.

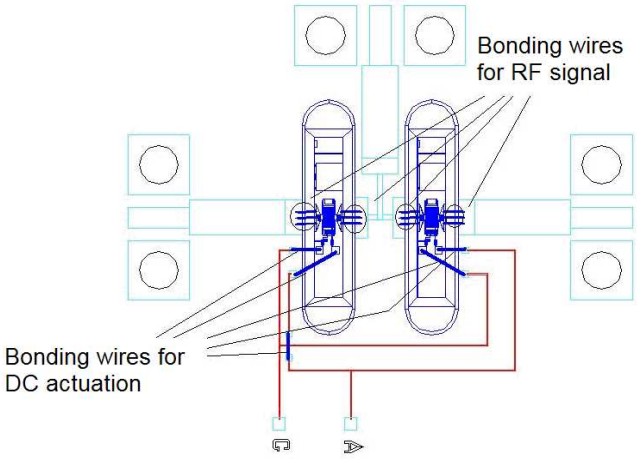

Fig. 2. Detail of the SPDT device. The bonding wires connections are evidenced by using text boxes.

First of all, to have a correct feeling of the SPDT expected best performances, ideal single switches have been realized by means of reference structures, simulating a device technologically actuated (bridge DOWN) or in the UP position. Being a series ohmic switch, the UP position of the bridge corresponds to the OFF state, while the DOWN position will correspond to the ON state. In particular, the OFF state has been obtained as a capacitive gap in the plane, without realizing the bridge in the central area of the single device, while the ON state has been obtained in two ways: (i) by using a geometry including a technologically actuated device, i.e. the switch without the sacrificial layer used for obtaining the real structure, and (ii) by means of a direct THRU, i.e. with a short microstrip line as long as the single switch. For both the technologically actuated configurations we shall use the definition DOWN-A and DOWN-B respectively.

SPDT ideal devices have been obtained by using the above procedure, for having the best experimental reference. Detailed photos of the three ideal SPST devices and their connections are given in Figs. 3–5. Actually, the utilization of DOWN-A and DOWN-B configurations will help in having a further confirmation on the quality of the shape chosen for the real device, in order to compare a simple microstrip line it with respect to the real fully actuated switch. In Fig. 6 the detail of an ideal SPDT including OPEN and DOWN-A devices.

For on-wafer measurement purposes, a TRL calibration kit has been implemented on alumina substrates, including the transition from microstrip to coplanar waveguide (CPW) by using THRU and LINEs having the shape given in the following Fig. 7, optimized for the (6–18) GHz band.

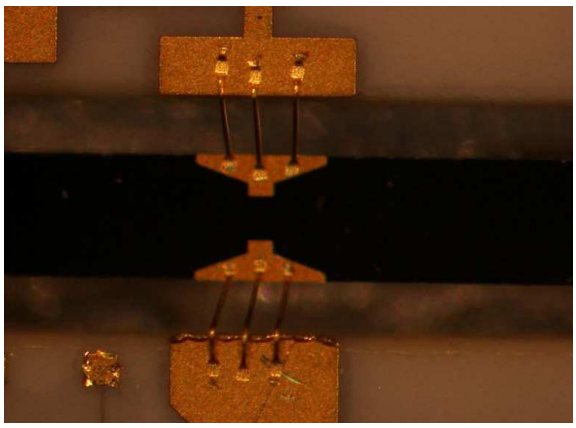

Fig. 3. OPEN structure used to simulate the ideal SPST in the OFF state and related I/O connections.

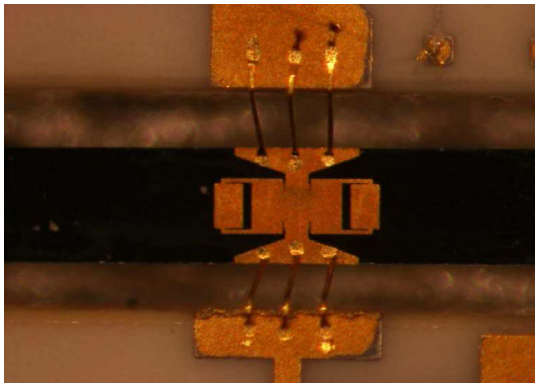

Fig. 4. Technologically actuated switch, used to simulate the ON state, realized without using a sacrificial layer in the process (DOWN-A).

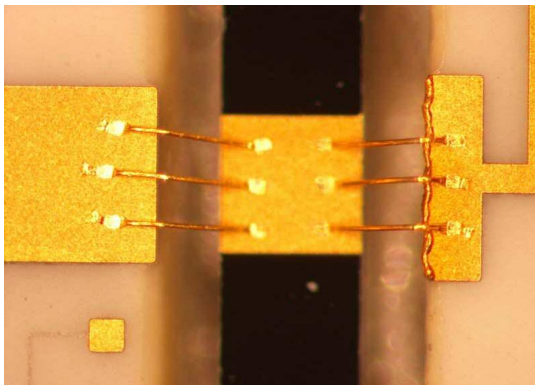

Fig. 5. Direct THRU simulating an ideal actuated SPST (DOWN-B device).

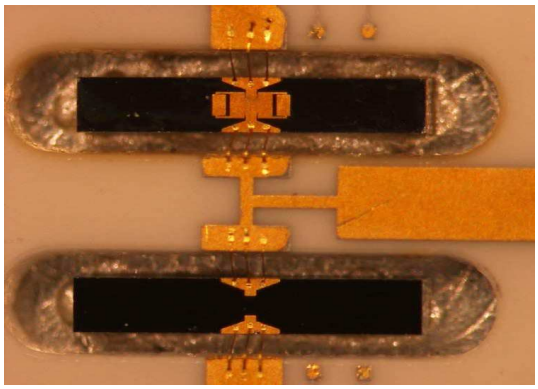

Fig. 6. Detail of the ideal SPDT obtained by using the OPEN and the DOWN-B devices.

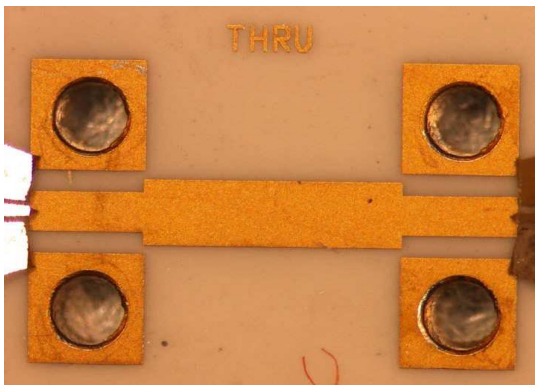

Fig. 7. THRU standard used for the TRL calibration needed for the G-S-G probes to be used for the on-wafer measurement.

The setup for the characterization of both ideal SPDT devices is shown in the following Fig. 8 and Fig. 9.

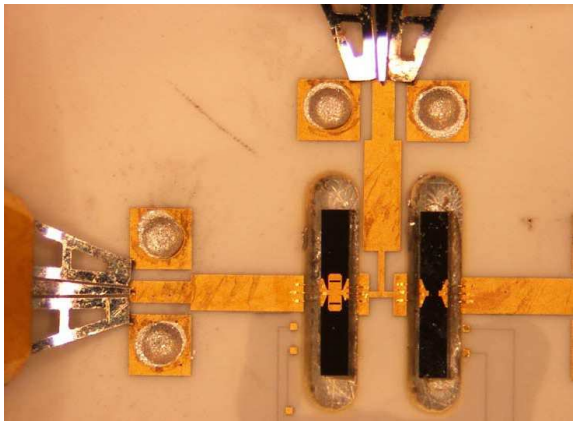

Fig. 8. Setup for measuring the ideal SPDT made by the OPEN and DOWN-A devices. The CPW probes positioning at the transition microstrip to CPW are also evidenced.

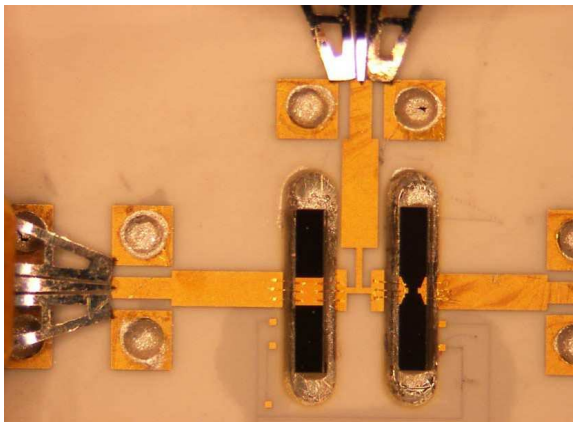

Fig. 9. SPDT with DOWN-B device, i.e. a short microstrip simulating the fully actuated switch, on the left, and the OPEN on the right.

The experimental results obtained for the device in Fig. 9 are shown in Fig. 10 and in Fig. 11, for the transmission, return loss and isolation on the second arm of the SPDT structure.

The results obtained with the DOWN-A device practically overlap the curves obtained in the previous figures.

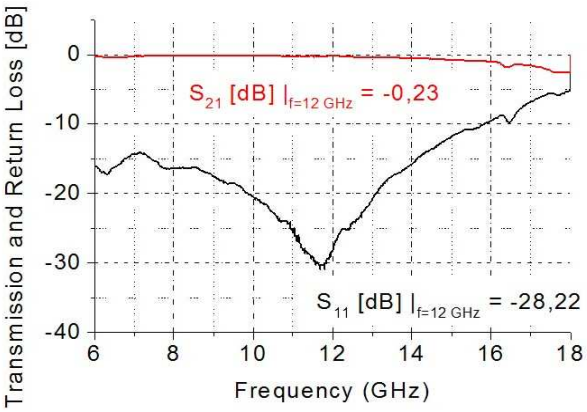

Fig. 10. Transmission and Return Loss of the SPDT realized by using the DOWN-B device, along the arm simulating the ON state.

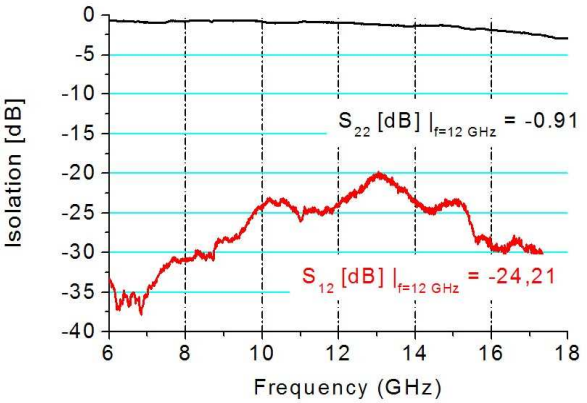

Fig. 11. Isolation measured on the SPDT based on the DOWN-B device, along the arm simulating the OFF state.

3. Alumina technology and true time delay line modules characterization

The TTDL has been designed by realizing the metallisation pattern on an alumina substrate 630 μm thick. Along the path, holes have been opened by laser processing to allow the positioning of the RF MEMS switches cut from the processed silicon wafer. The thickness for alumina has been chosen to be as close as possible to the commercial silicon substrate used for manufacturing the single switches. In fact by using this solution, short wires have been used for connecting the switches.

TRL standards useful for the calibration, SPDT and TTDL have been all realized by using the mask shown in Fig. 12. In Fig. 13 the devices to be realized on silicon to get the ideal OPEN, DOWN-A and DOWN-B structures are also shown, obtained by

partially using the mask in Fig. 12. In the following figures, the assembling procedure for obtaining the TTDL structure (Fig. 14) and details on the wire bonding needed to connect the RF MEMS switches to the TTDL layout (Fig. 15) are shown. In Fig. 16, the single SPST connected device is also shown, to be compared with the assembling presented in Fig. 3–5. The packaging scheme is given in Fig. 17, where details about the assembling, wire bonding, substrates used, transitions and cover positioning are also given.

A cross section of the wire bonding is shown in Fig. 18.

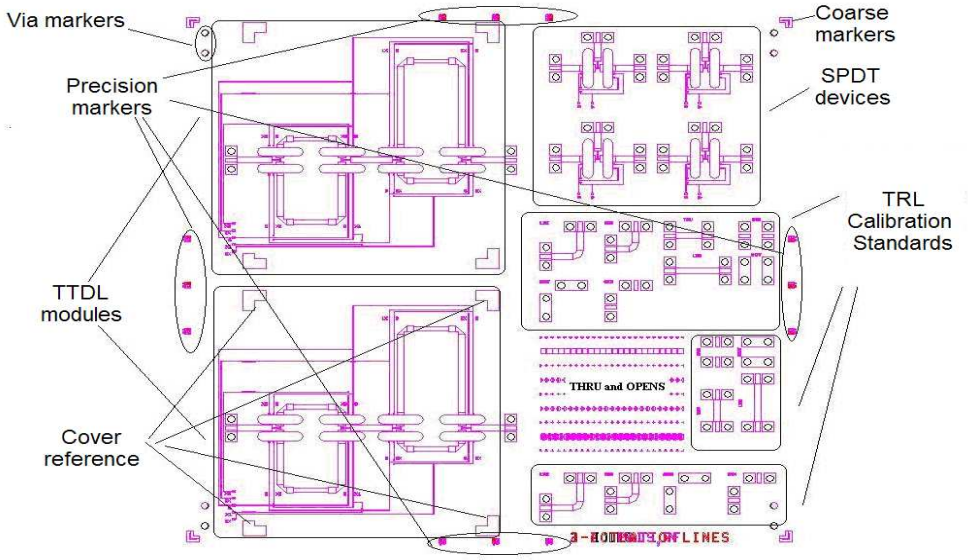

Fig. 12. General view of the mask layout, where space for the THRU and OPEN devices to be realized onto the silicon wafer have been also considered.

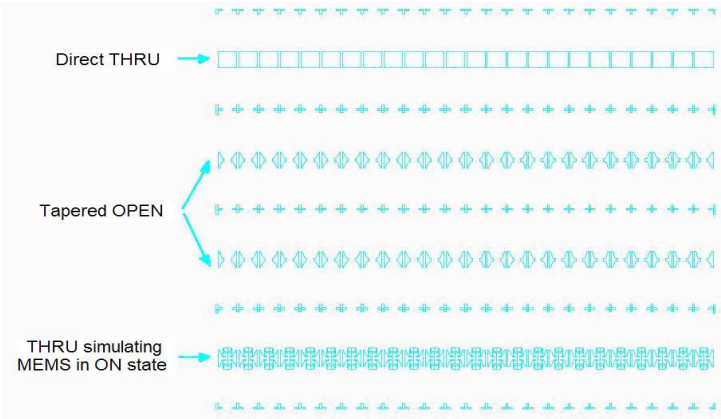

Fig. 13. Detail of the Silicon THRU and OPEN simulating the ON and OFF states respectively.

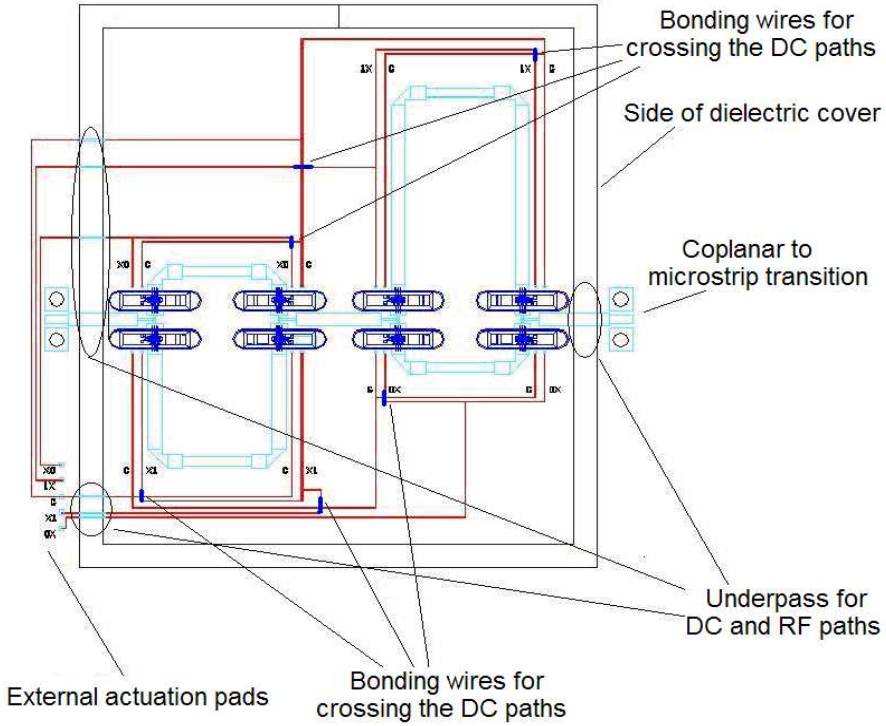

Fig. 14. General view of the TTDL module with the switches in the holes obtained by laser processing.

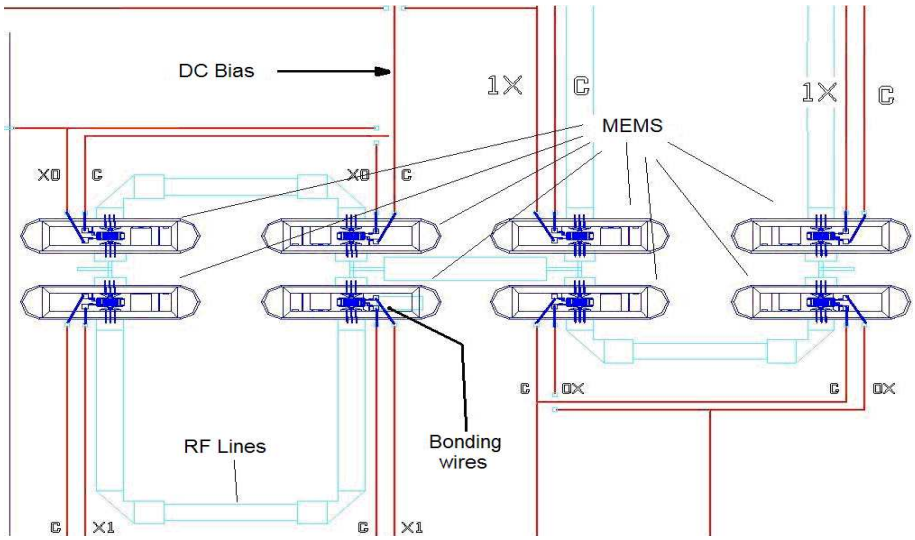

Fig. 15. Zoom of the TTDL module in the region of the MEMS cavities.

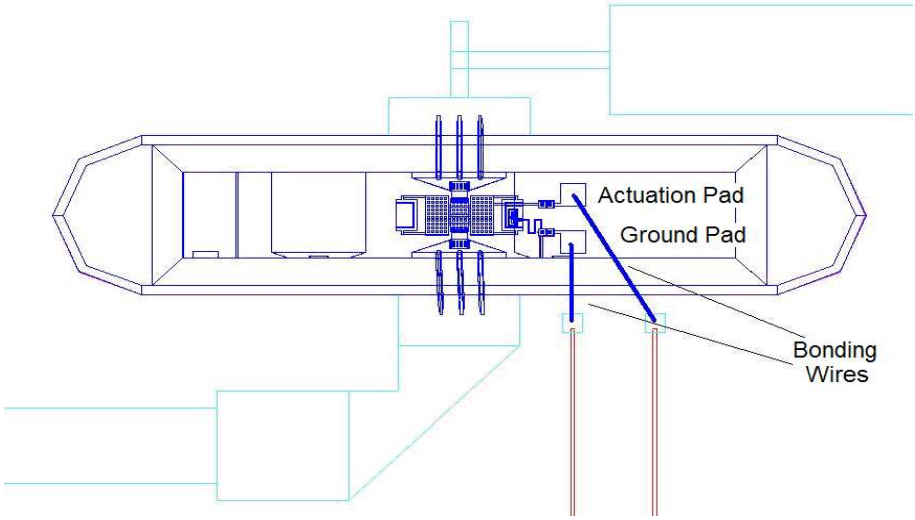

Fig. 16. Detail of one of the wire bonding connection from the DC pads of the MEMS in the cavities with the feeding lines on alumina.

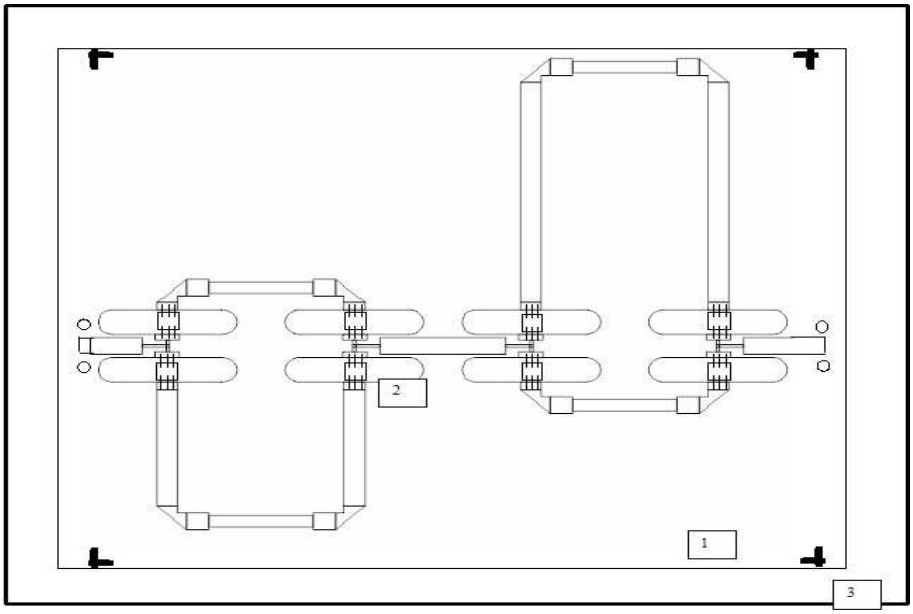

Fig. 17. General assembly of the TTDL module to be packaged. In particular, 1 is the alumina substrate, 2 are the places for MEMS positioning (8 all together) and 3 the metal support for the alumina package. The cover has to be placed on the four corners indicated in the figure. To provide the proper ground connection for the SPST a conductive epoxy on the back side has been used.

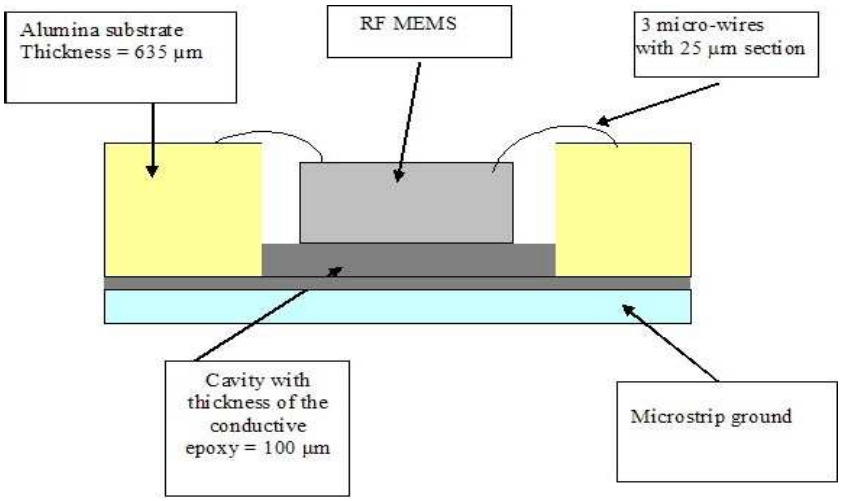

Fig. 18. Wire bonding of the SPST RF MEMS in the alumina environment. The optimal dimensions obtained by using electromagnetic simulations are given. In particular, the best predictions on the SPST response have been obtained with the wires as short as possible, which practically impose to have the silicon wafer as thick as the alumina substrate.

In the following plots, the measurements on TTDL having ideal devices mounted (i.e. OPEN, DOWN-A and DOWN-B) are presented. Specifically, as a reference, the short path of the device and the long path have been assembled and measured. In Figs. 19–21 the electrical response of the shortest path obtained by using the DOWN-A solution (technologically actuated MEMS) is presented. In Figs. 22–24 the device DOWN-A has been used for the longest path structure. In Figs. 25–27 the device DOWN-B has been used for the same purposes.

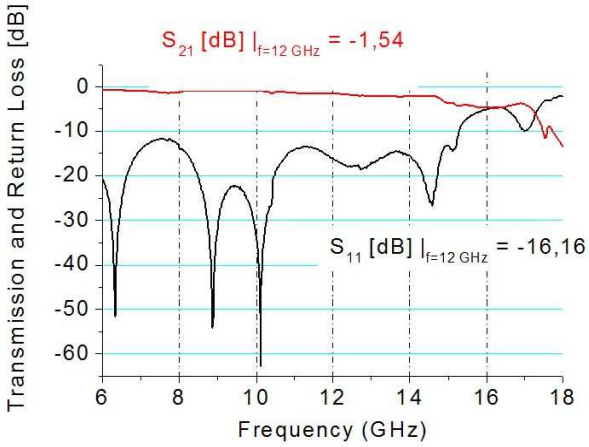

Fig. 19. TTDL Transmission and Return Loss, short path with device DOWN-A.

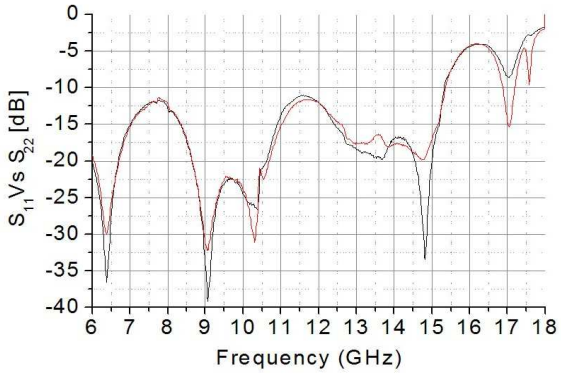

Fig. 20. Return Loss of the TTDL, short path with device DOWN-A, measured on both I/O ports to check the symmetry of the device response.

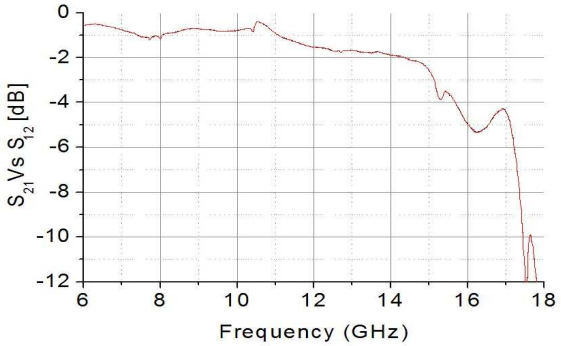

Fig. 21. Insertion Loss for the TTDL, short path with device DOWN-A, transmission along both directions. S_{12} and S_{21} are perfectly overlapped.

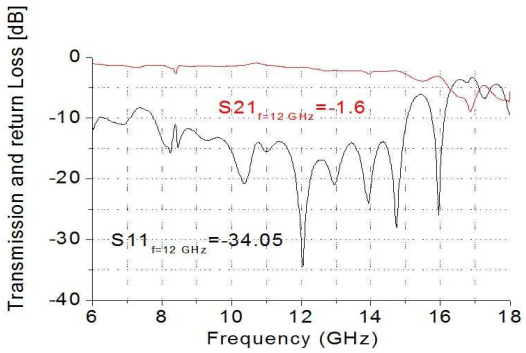

Fig. 22. Return Loss and Transmission for the TTDL, long path with device DOWN-A.

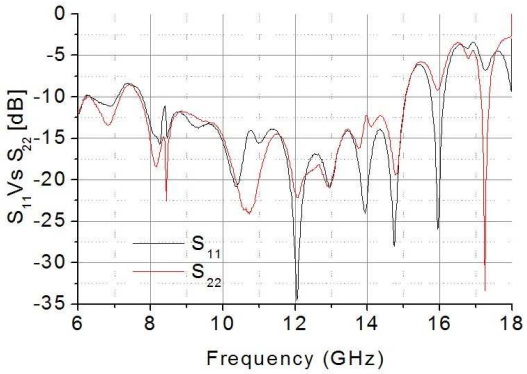

Fig. 23. Return Loss for the TTDL, long path with device DOWN-A.

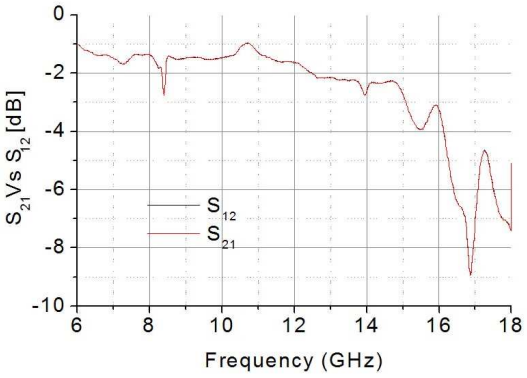

Fig. 24. Transmission response for the TTDL, long path with device DOWN-A.

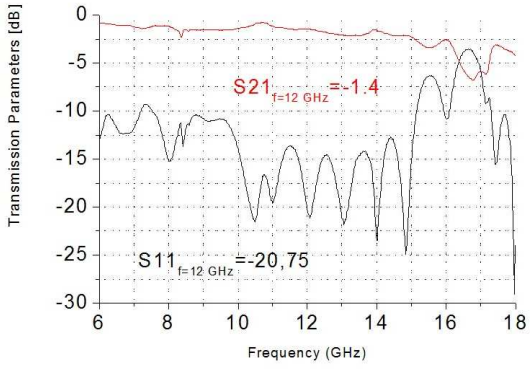

Fig. 25. Return and Insertion Loss for the TTDL, long path with device DOWN-B.

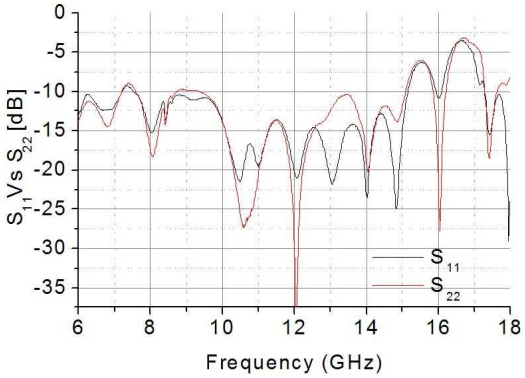

Fig. 26. Return Loss for the TTDL, long path with device DOWN-B.

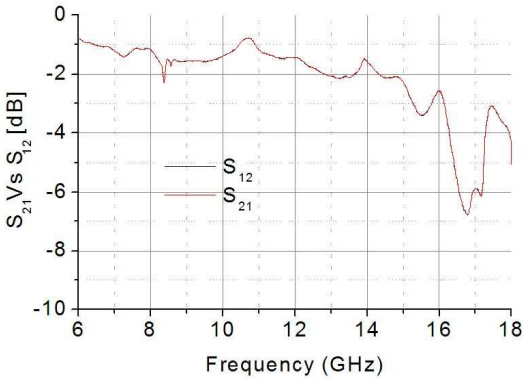

Fig. 27. Transmission response for the TTDL, long path with device DOWN-B.

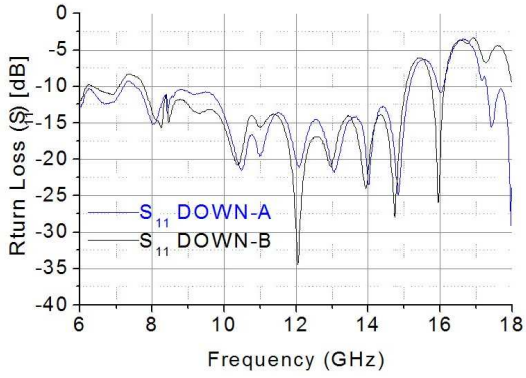

Fig. 28. S_{11} Return Loss for TTDL long path by using devices DOWN-A and DOWN-B.

From the comparison between the two possible solutions for the ideal reference device, both DOWN-A and DOWN-B have practically the same response. The curves with the results coming from the characterization of TTDL based on the two reference devices are plotted in Figs. 28–30.

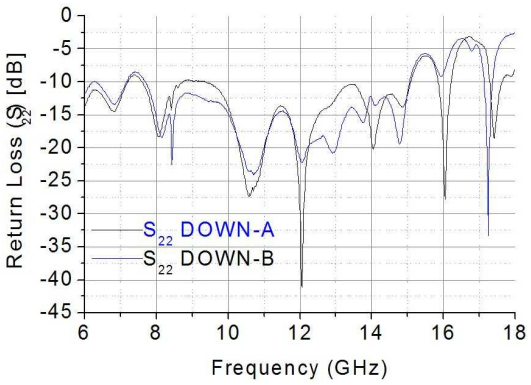

Fig. 29. S_{22} Return Loss for TTDL long path by using devices DOWN-A and DOWN-B.

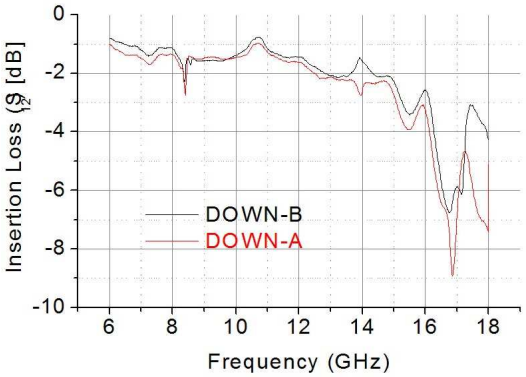

Fig. 30. Insertion Loss of the ideal TTDL, long path, with devices DOWN-A and DOWN-B.

4. Delay time measurements on the ideal structures

The Scattering Parameters measurements have been used for the evaluation of the delay times for the TTDL. By using the data coming from the curves of the previous sections, the delay time T_d has been calculated as $T_d = -\frac{1}{360}\frac{\partial\phi\,[\mathrm{deg}]}{\partial f}$, and it has been plotted in the following Figs. 31–32 for the absolute paths and for the differential delay time, i.e. T_d(long path)-T_d(short path).

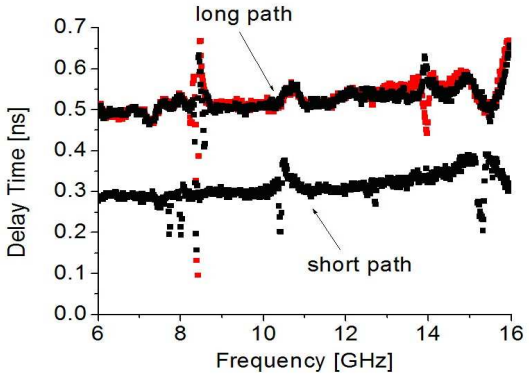

Fig. 31. Delay time for the short path and for the long path of the technologically actuated TTDL. The red and black curves on the upper part of the plot, almost superimposed, correspond to the devices DOWN-A and DOWN-B respectively, while for the short path the device DOWN-A has been used.

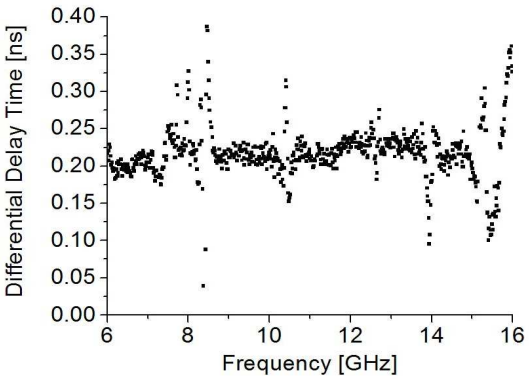

Fig. 32. Differential delay time as a difference between the long and the short path of the measured technologically actuated TTDL.

5. Experimental results on the real TTDL structures

After the evaluation of the TTDL configurations by using technologically actuated devices, real structures, i.e. containing the RF MEMS switches to be actuated, have been assembled. Some differences have been experienced with respect to the reference structures, but with encouraging results indicating the necessary implementations of the building blocks of the TTDL. First of all, the actuation voltage V_{act} for the TTDL configurations is always higher than that used for the single switch to get the expected change of the scattering parameters and, consequently, in the delay time performances. Actually, V_{act} is in the order of 40–45 volt for the individual device,

but voltages as high as 80–100 volt are necessary to obtain the full actuation of the paths for the TTDL structure. A possible reason for such a difference could be in the feeding lines, which have been designed for quite long paths with respect to the single switch, and both the high resistivity (from 20 to 50 kΩ) and an excessive length could be the reason for a drop of voltage along the line. Moreover, real devices can suffer for contact resistances as high as few ohm, al already stressed in the measurement results performed on the single switch. For this reason, considering four MEMS involved in the definition of the long path, almost 1.6 dB more in the insertion loss is expected with respect to the technologically actuated configuration. From the analysis of the following Fig. 33 and Fig. 34 an encouraging result is obtained in terms of the isolation, which is around 40 dB for the entire structure before the application of the voltage, while the insertion loss, when a voltage of 80 volt is applied, is around 4.5 dB at 12 GHz, i.e. 1.5 dB ca. more with respect to the ideal structure, as expected from the utilization of the real MEMS.

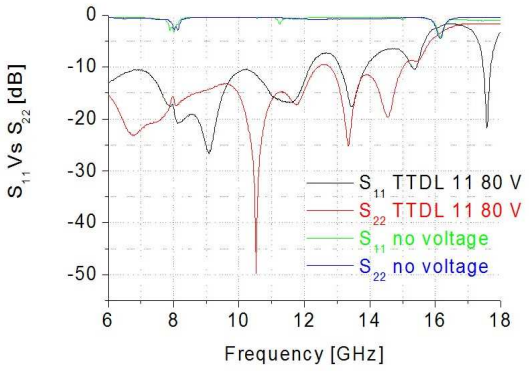

Fig. 33. TTDL long path Return Loss before the actuation (no voltage) and after imposing a 80 volt actuation voltage.

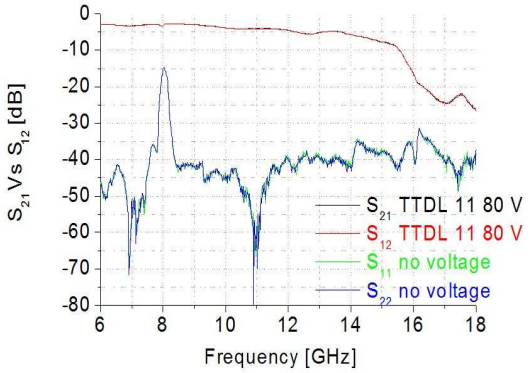

Fig. 34. TTDL long path Transmission response before the actuation (no voltage) and after imposing an 80 volt actuation voltage.

Moreover, no change in the electrical performances has been recorded by repeating the actuation at least ten times, as evidenced in Fig. 35, where the curves are exactly superimposed after the first measurement and after the tenth one. A more stressing reliability test will be also performed for this structure. In Fig. 36, the comparison between the reference, technologically actuated TTDL has been plotted and the real structure, evidencing a significant change after 14 GHz. The delay time, to be compared with the results for the ideal structure, is given in Fig. 37, where both the real and technologically actuated structure responses have been plotted.

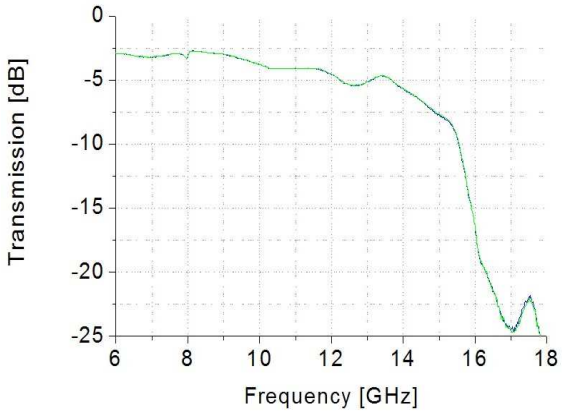

Fig. 35. TTDL long path. A limited reliability test has been performed, and after ten actuations no change in the electrical performances has been recorded.

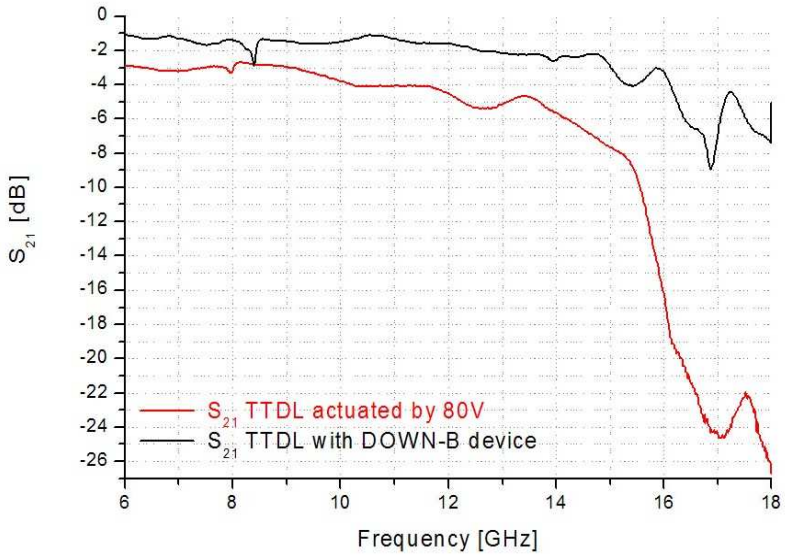

Fig. 36. Comparison between the ideal, technologically actuated TTDL (long path) and the real one.

The short path of the TTDL has been also measured by using the real devices, and it turned out the result in Fig. 38, while in Fig. 39 the delay time has been plotted.

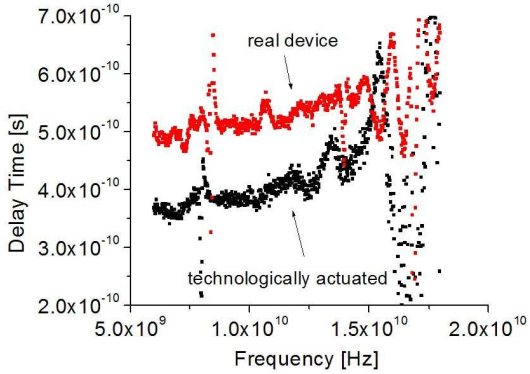

Fig. 37. Delay Time for technologically actuated TTDL, long path, and for the really actuated one.

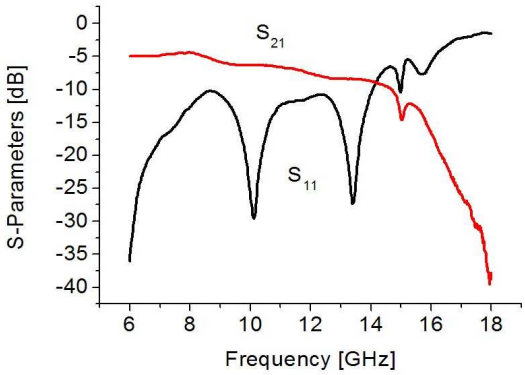

Fig. 38. S-parameters for the TTDL, short path.

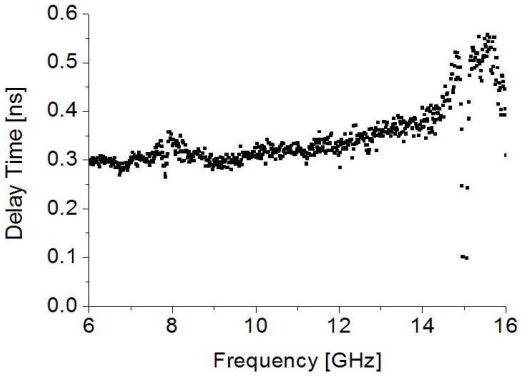

Fig. 39. Delay Time for the TTDL short path.

As a final comparison between the two real structures, the delay times for both paths measured on real structures is shown in the following Fig. 40.

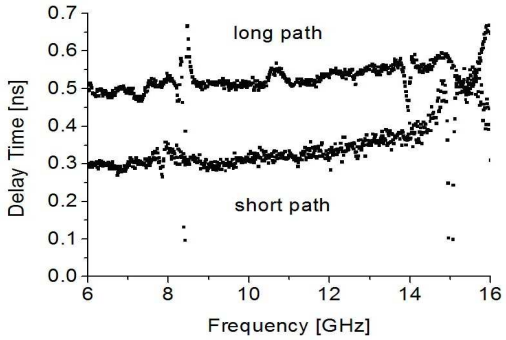

Fig. 40. Delay Time for the TTDL short path and long path measured on the real devices.

6. Simulations

The expected response of the investigated TTDL structures has been obtained simulating the short path and the long path configurations by means of electromagnetic and circuital approaches. Actually, the electrical response of the packaged SPST has been predicted accounting for its real dimensions inside the hole realized into the alumina substrate, including the wire bonding connections for the I/O lines. In such a simulation, the HFSS package has been used. After that, the S-parameters of the building block in the ON and OFF states have been used to define *black boxes* for circuital simulations by means of Microwave Office, connecting the SPSTs by means of microstrip lines on an alumina substrate. The expected results are shown in Fig. 41 and in Fig. 42 for the short and for the long path respectively and in Fig. 43 in the case of the transmission parameter for both of them.

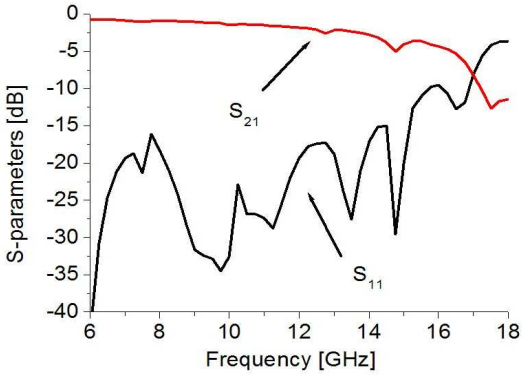

Fig. 41. Simulated S-Parameters for the short path of the TTDL.

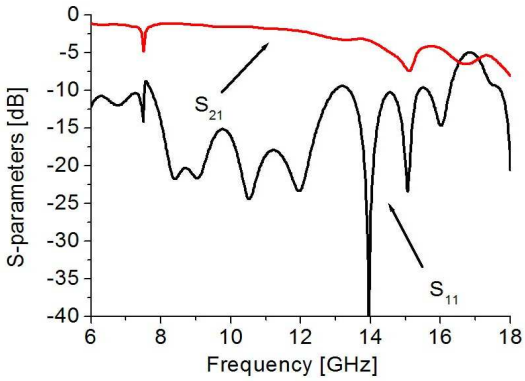

Fig. 42. Simulated S-Parameters for the long path of the TTDL.

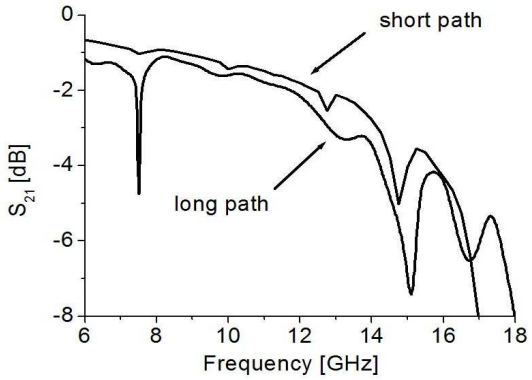

Fig. 43. Comparison of the simulated transmission for the short and for the long path of the TTDL.

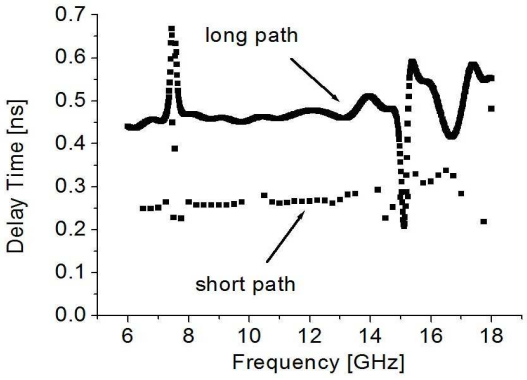

Fig. 44. Expected delay time for the short and for the long path of the TTDL.

From the analysis of the above figures it turns out that, further to the obviously lower losses, a better electrical matching is expected for the short path, as evidenced by the low frequency response and by the less pronounced peaks in the transmission.

The presence of the peaks is the cause of some oscillations in the delay time, as shown in Fig. 44.

The simulation of the delay time is in quite good agreement with the measured one for both structures, as from the comparison between results presented in Fig. 40 and in Fig. 44, especially concerning the differential delay time, which is in the order of 0.2 ns over the entire frequency range, as also measured on the real structures. Of course, in the simulation the mismatch effects are less evident than in the real case, but they are always present, causing the notches predicted in Fig. 43. It is reasonable to assume that the investigated structures need a further optimization to avoid reflections due to stubs and or additional wires. In fact, the TTDL has been realized by implementing SPSTs as the building blocks of the entire system. We believe that by using SPDTs as elementary units the losses can be decreased, and the SPSTs can be realized more close each other, thus positively influencing the reduction in the reflections to get a more flat response of the differential delay time vs. frequency.

7. Actuation time evaluation

From energetic considerations, in the case of a shunt capacitive RF MEMS switch close to the full actuation, we can write:

$$\begin{aligned} &\frac{1}{2}C_{OFF}V^2 = \frac{1}{2}kg^2 + E_k + E_d = \\ &\frac{1}{2}kg^2 + \frac{1}{2}mv^2(\tau_{act}) + \frac{\beta}{\omega}v^2(\tau_{act}) = \\ &\frac{1}{2}kg^2 + \frac{1}{2}v^2(\tau_{act})\left(m + \frac{2\beta}{\omega}\right), \end{aligned} \tag{1}$$

where C_{OFF} is the capacitance in the OFF state (down position of the bridge), E_k is the kinetic energy and E_d the dissipated one, m is the bridge mass in the central area, k is the spring constant, g the gap between bridge and substrate, while $\omega = \sqrt{k/m}$. The dissipated energy has been calculated accounting for the dissipated power $P_d = Fv = \beta v^2 = \omega E_d$. All is valid under the assumption that we are very close to the full actuation of the switch, but far enough to be obliged in considering the Van Der Waals and contact contributions. This is the reason why the capacitance has been chosen as C_{OFF}, i.e. the value of C when the switch is actuated. From Eq. (1) it turns out that the velocity v of the bridge subjected to the force exerted by means of the applied voltage is linearly dependent on the voltage V. So far, Eq. (2) describes the energy an instant before the bridge is collapsed. We can also write:

$$v^2 = \frac{C_{OFF}V^2 - kg^2}{m + 2\dfrac{\beta}{\omega}} \quad \rightarrow \quad \left(\frac{C_{OFF}V^2 - kg^2}{m}\right)_{\beta\rightarrow 0}. \tag{2}$$

Actually, the dissipation causes a decrease in the velocity of the actuation by means of a term depending on β. It is like to substitute the mass of the bridge m with $m' = m + (2\beta/\omega)$. With this finding, the actuation time can be obtained accounting that:

$$v(t) = \dot{z}(t) = \frac{d}{dt}\left(d + g\exp\left(-\frac{\beta}{2}t\right)\right). \tag{3}$$

And it turns out that the actuation time is:

$$\tau_{act} = -\frac{1}{\beta}\ln\left(\frac{4}{\beta^2 g^2}\frac{C_{OFF}V^2 - kg^2}{m + 2\dfrac{\beta}{\omega}}\right). \tag{4}$$

In the case of an ohmic resistive configuration, the situation is a bit different, because the equivalent circuit in the OFF state (bridge UP, signal inhibited) will be the capacitive gap along the interrupted line under the bridge, and in the ON state (bridge DOWN, signal passing) resistive and inductive contributions have to be considered. On the other hand, if a lateral actuation is performed by using dielectric pads, we shall have a capacitance defined by a poly-silicon pad and the metal bridge with SiO_2 as a dielectric. It means that Eq. (4) can be re-written by using C_{pad} instead of C_{OFF}, as the voltage is used to close this circuit in DC to allow the RF passage through the collapsed metal bridge:

$$\tau_{act} = -\frac{1}{\beta}\ln\left(\frac{4}{\beta^2 g^2}\frac{C_{pad}V^2 - kg^2}{m + 2\dfrac{\beta}{\omega}}\right). \tag{5}$$

The pads used for the device under test have an area A=120×120 μm^2, and a dielectric thickness $d = 0.3$ μm, and it will be C_{pad} ≈8.85×10^{-12}×3.94×120^2×10^{-6}/0.3 ≈1.7 pF.

By using Eq. (5) and accounting that $g = 1.5$ μm, the threshold voltage can be calculated as $V_{threshold} = 47$ volt ca.. By changing the applied voltage starting from the threshold value, the following plot of the actuation time Vs. the applied voltage can be obtained (see Fig. 45).

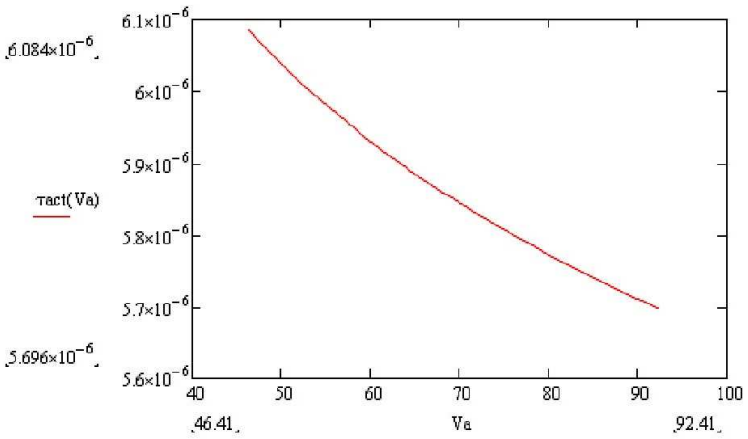

Fig. 45. Actuation time τ_{act} (in s) vs. the applied voltage V_a (in volt). For the exploited configuration $\tau_{act} \approx 6\mu s$ can be estimated for the single switch.

8. Conclusions

SPDT and TTDL structures based on RF MEMS switches have been designed, realized and tested in packaged configurations obtained by embedding the SPST in an alumina structure, where the paths have been properly defined. Differential delay times within 0.2 ns have been obtained in the frequency range (6–18) GHz.

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